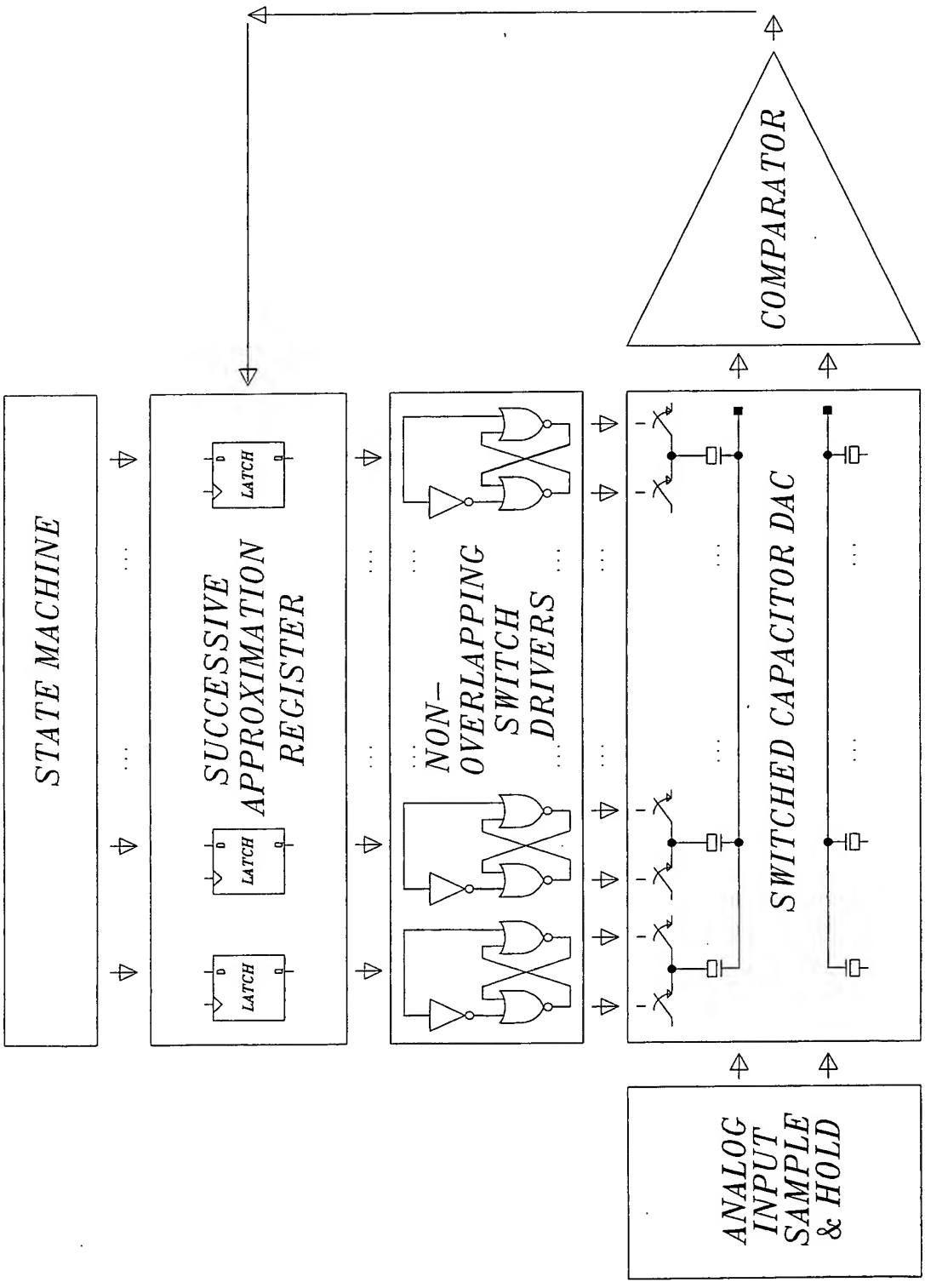

Fig. 1 (Prior Art)

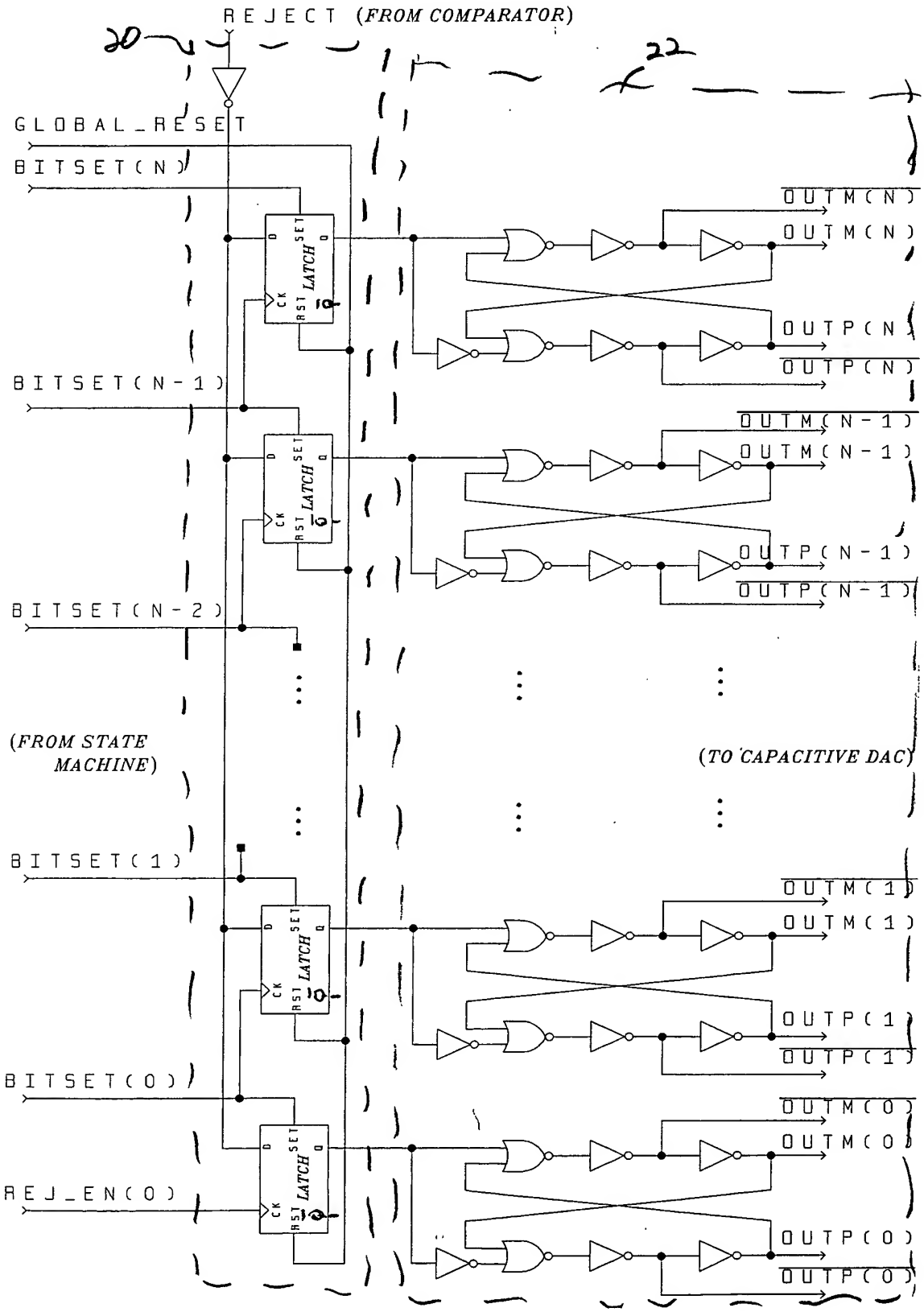

Fig. 2 (Prior Art)

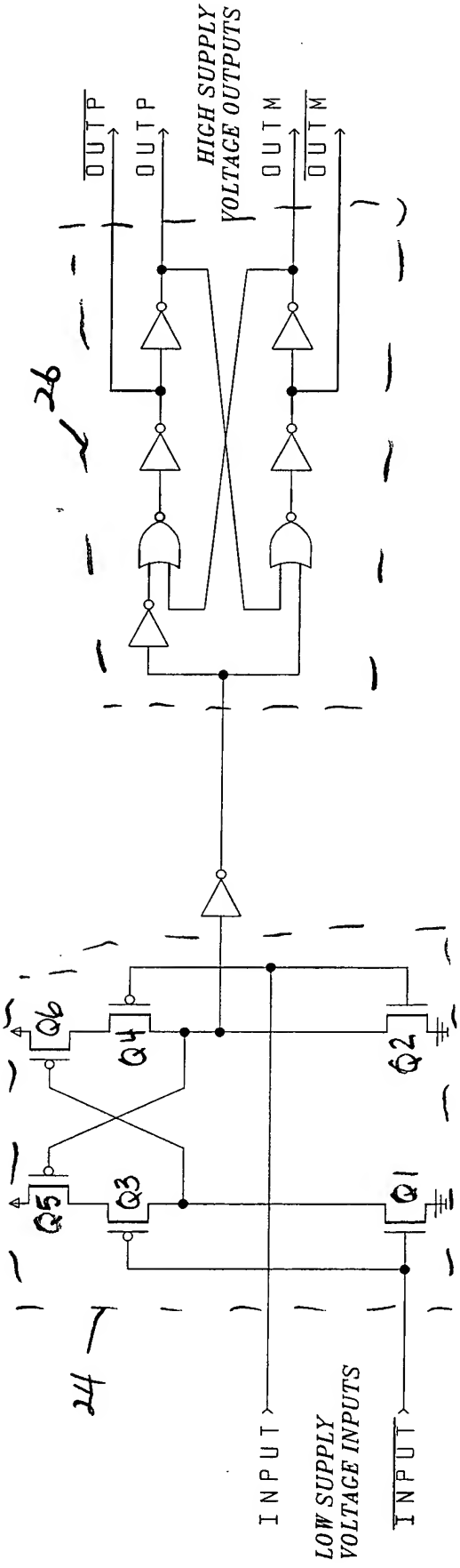

Fig. 3 (Prior Art)

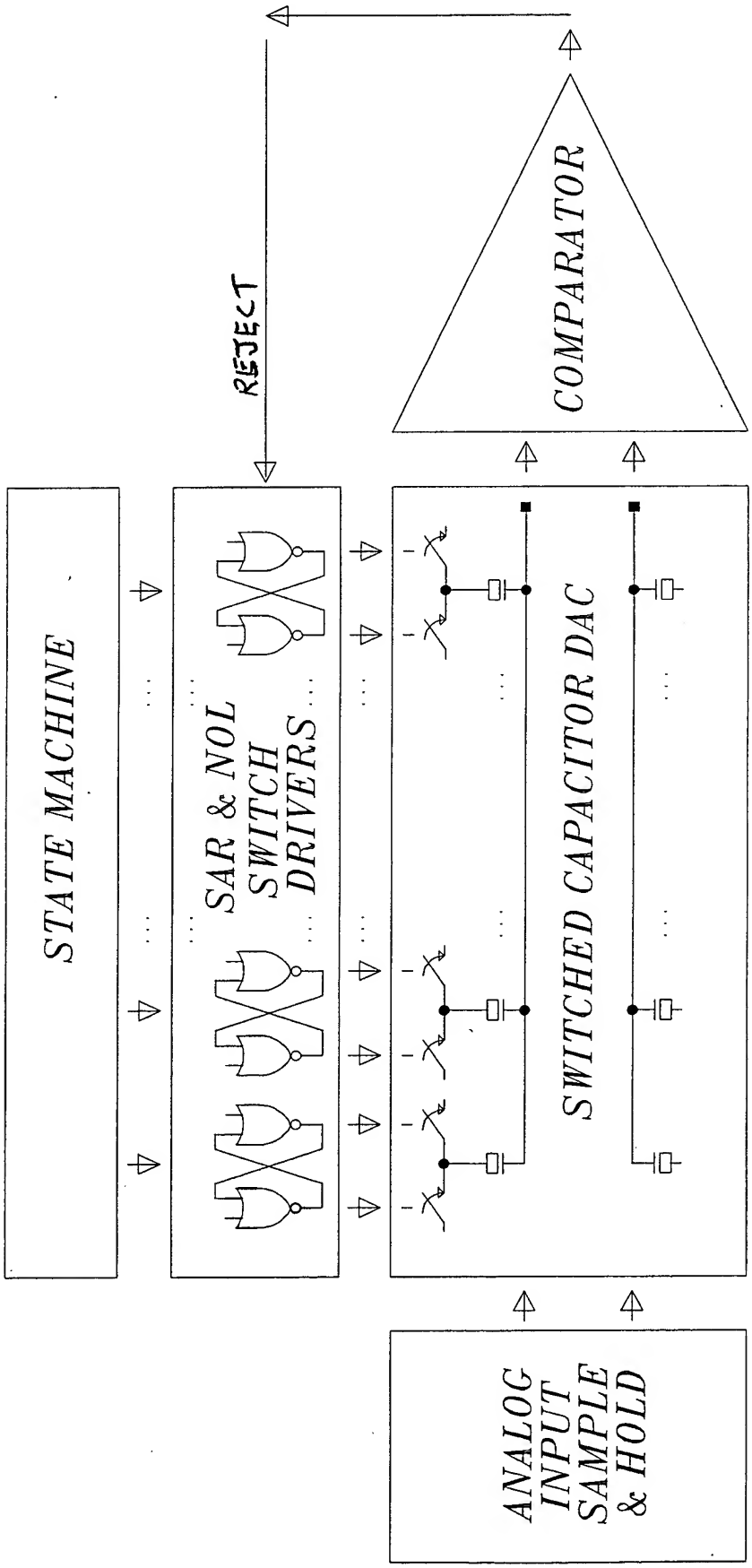
REJECT
COMPARATOR
STATE MACHINE
SAR & NOL SWITCH DRIVERS
SWITCHED CAPACITOR DAC
ANALOG INPUT SAMPLE & HOLD

Fig. 4

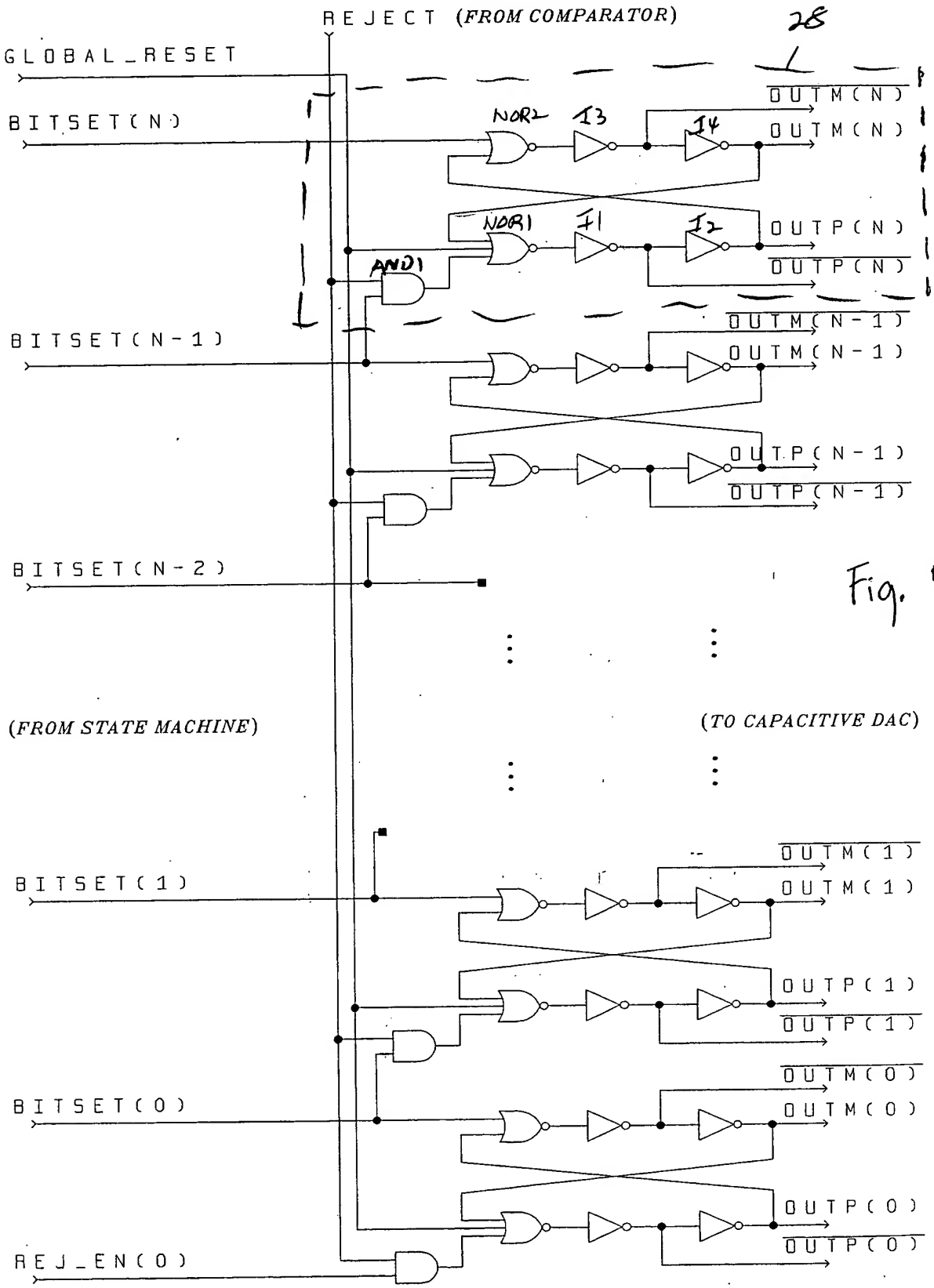
REJECT (FROM COMPARATOR)
28
GLOBAL_RESET
BITSET(N)
NOR2
I3
I4
OUTM(N)
OUTM(N)
NOR1
I1
I2
OUTP(N)
OUTP(N)
AND1
BITSET(N-1)
OUTM(N-1)
OUTM(N-1)
OUTP(N-1)
OUTP(N-1)
BITSET(N-2)
(FROM STATE MACHINE)
(TO CAPACITIVE DAC)
BITSET(1)
OUTM(1)
OUTM(1)
OUTP(1)
OUTP(1)
BITSET(0)
OUTM(0)
OUTM(0)
OUTP(0)
OUTP(0)
REJ_EN(0)

Fig. 5

NOR BASED SET–RESET LATCH

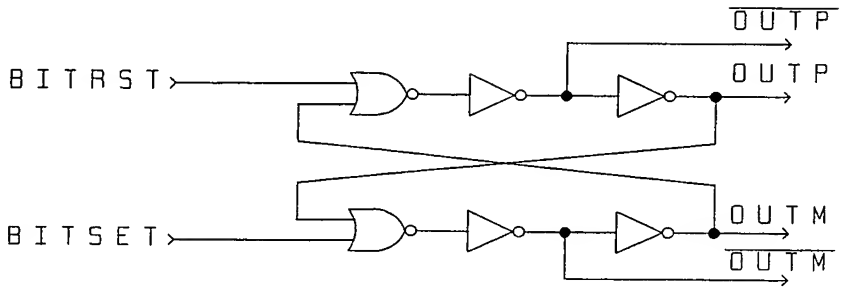

Fig. 6a

NAND BASED SET–RESET LATCH

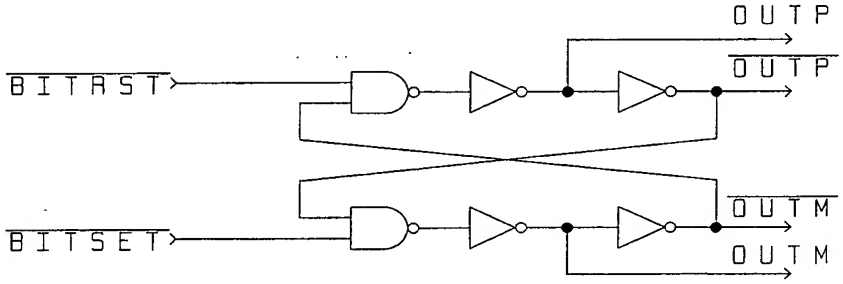

Fig. 6b

NAND BASED SET–RESET LATCH WITH SET & RST ENABLES

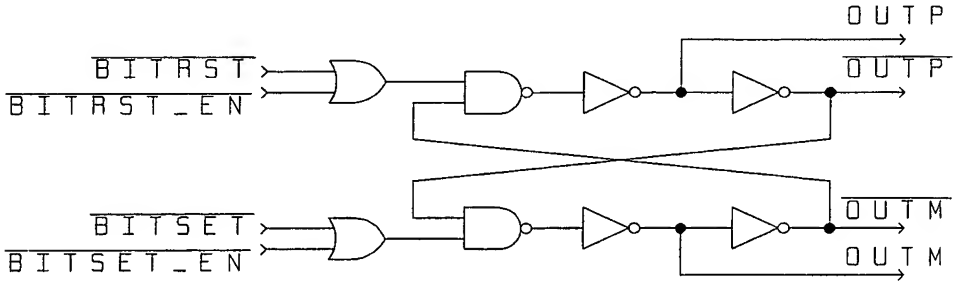

Fig. 6c

NOR BASED SET–RESET LATCH WITH RST ENABLE & GLOBAL RST

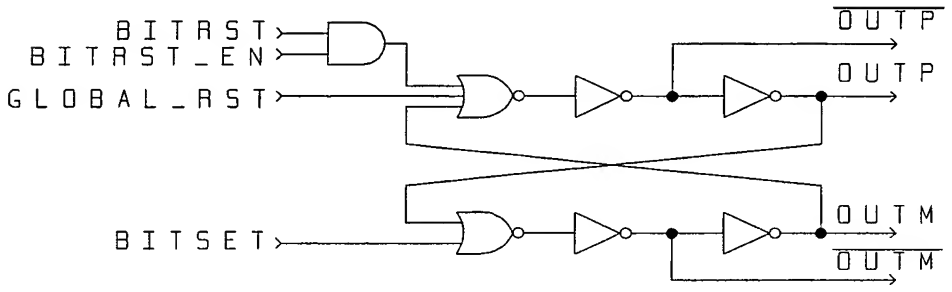

Fig. 6d

NOR BASED SET–RESET LATCH WITH RST ENABLE & GLOBAL RST USING COMPOUND AOI GATE

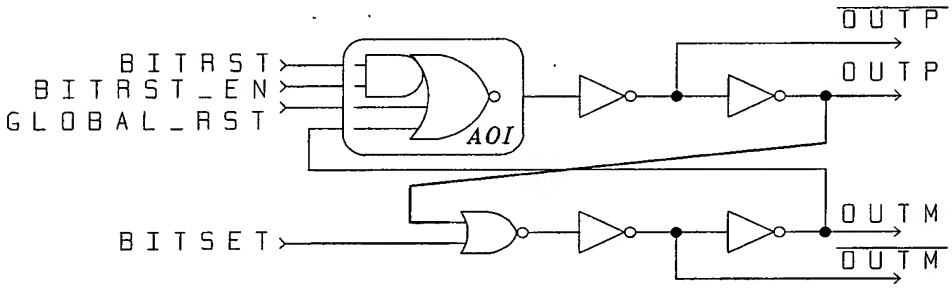

Fig. 6e

NOR BASED SET–RESET LATCH WITH RST ENABLE & GLOBAL SET & RST USING COMPOUND AOI GATE

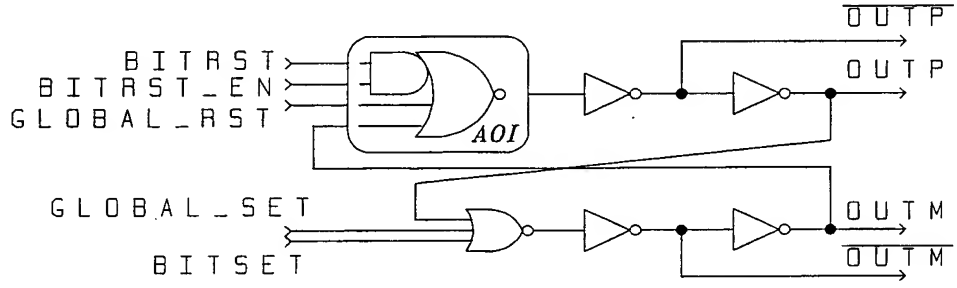

Fig. 6f

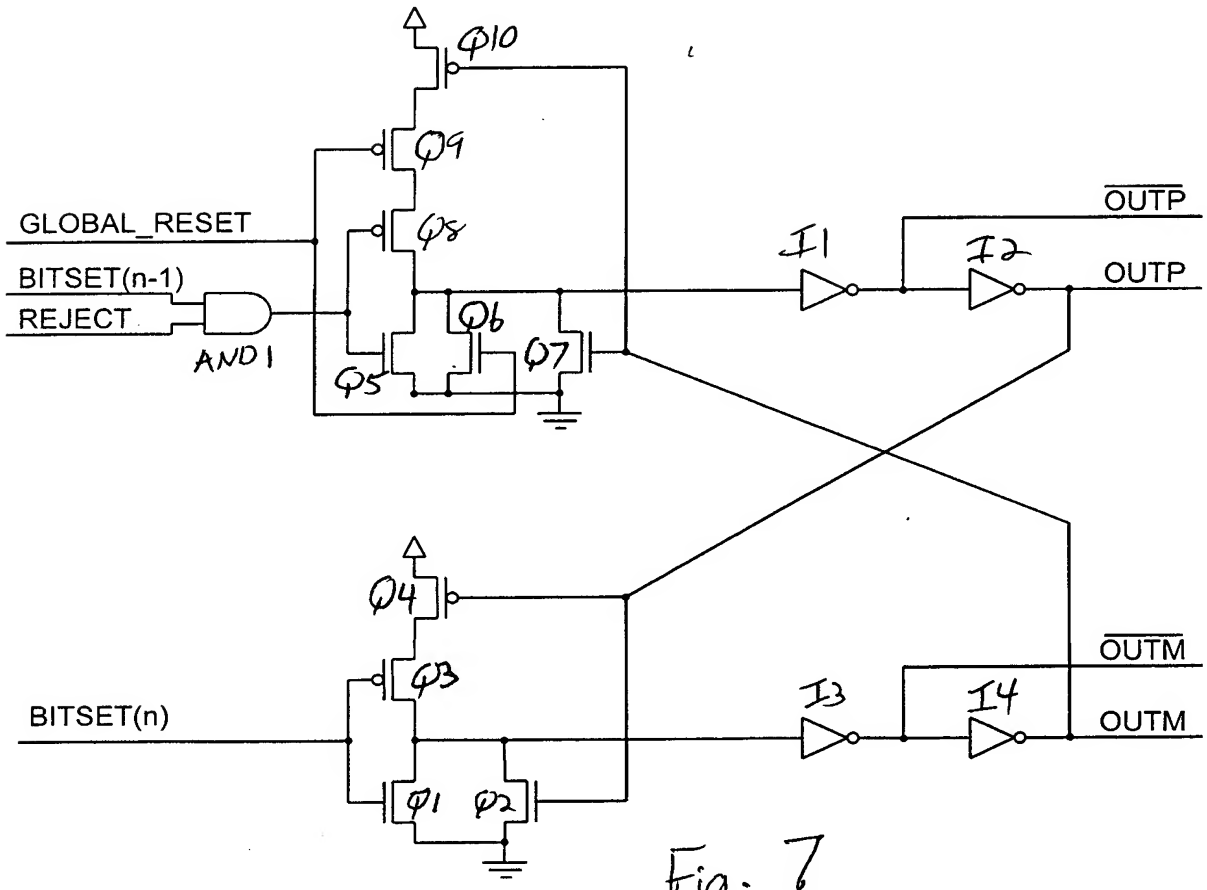
Q10
Q9
Q8
GLOBAL_RESET
BITSET(n-1)
REJECT
AND1
Q6
Q7
Q5
I1
I2
OUTP
OUTP
Q4
Q3
BITSET(n)
Q1
Q2
I3
I4
OUTM
OUTM

Fig. 7

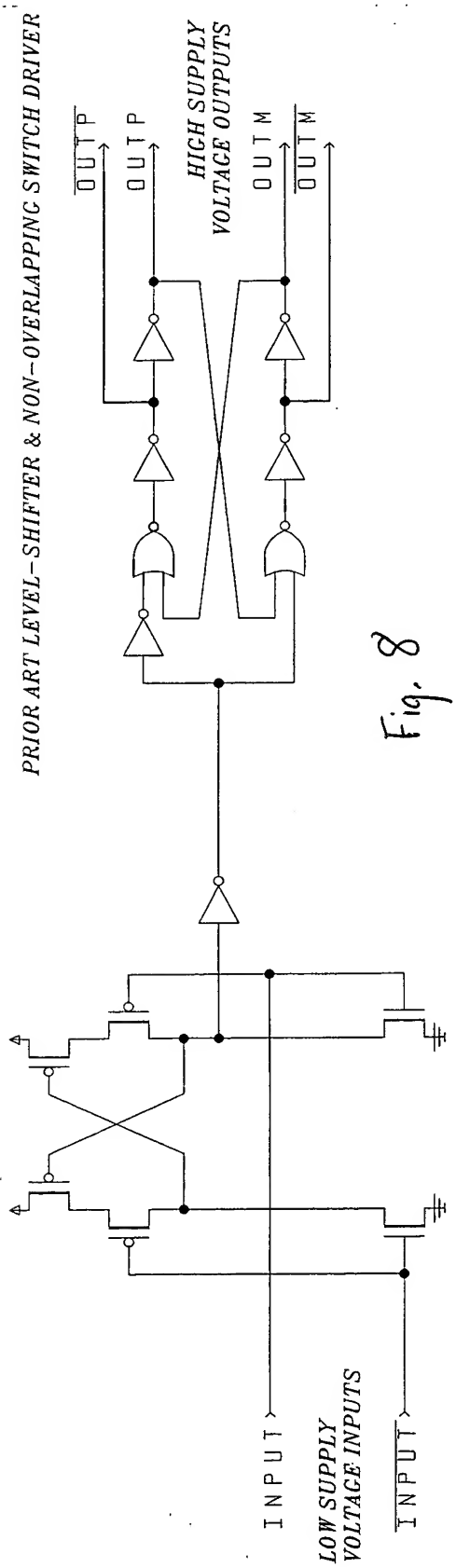
PRIOR ART LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
HIGH SUPPLY VOLTAGE OUTPUTS
OUTP
OUTP
OUTM
OUTM
INPUT
INPUT
LOW SUPPLY VOLTAGE INPUTS

Fig. 8

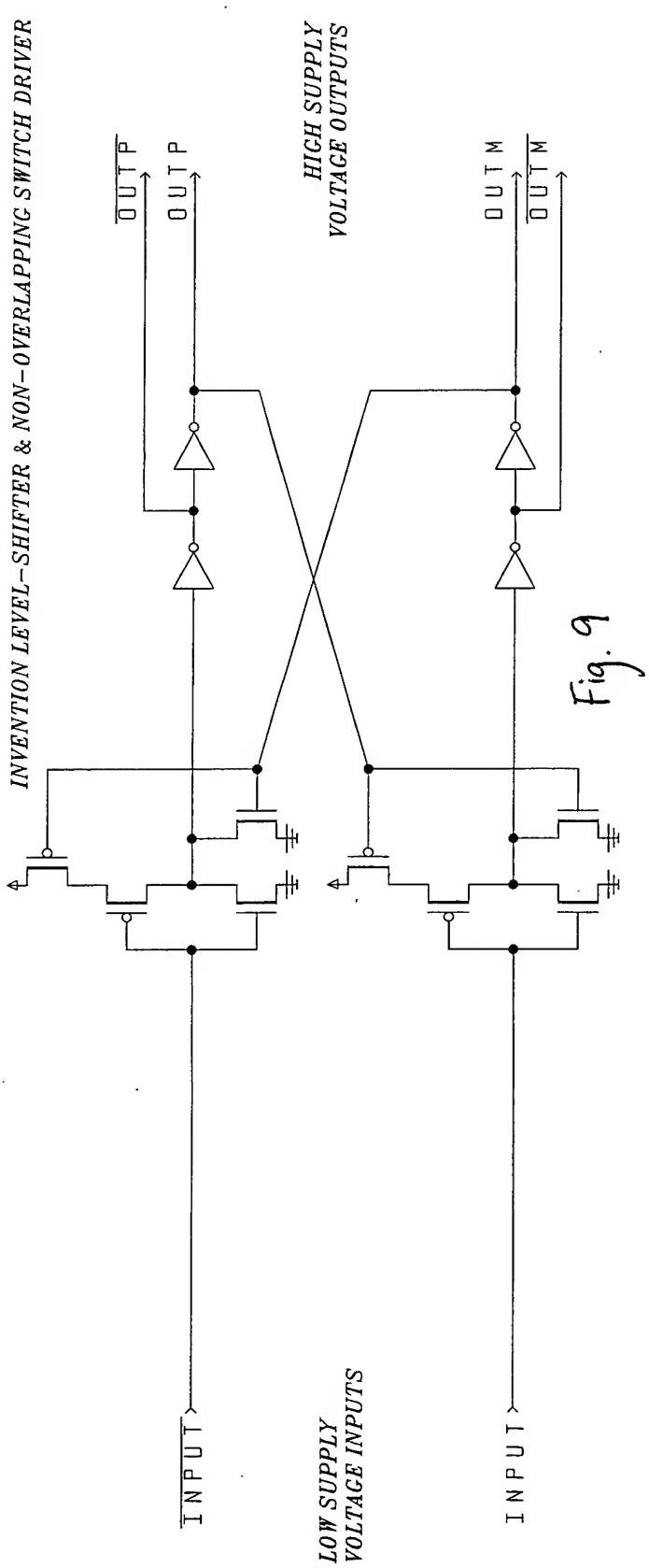
INVENTION LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
HIGH SUPPLY VOLTAGE OUTPUTS
OUTP
OUTP
OUTM
OUTM
INPUT
INPUT
LOW SUPPLY VOLTAGE INPUTS

Fig. 9

PRIOR ART LATCH & NON-OVERLAPPING SWITCH DRIVER

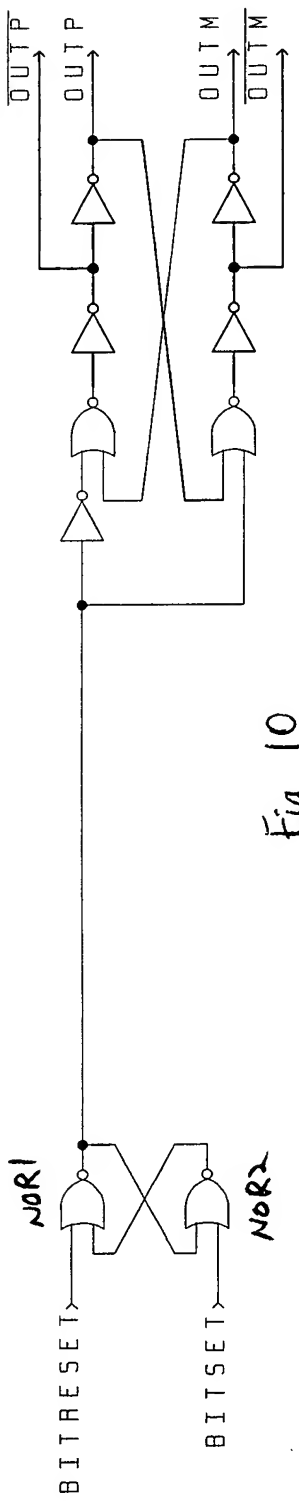

Fig. 10

INVENTION LATCH & NON-OVERLAPPING SWITCH DRIVER

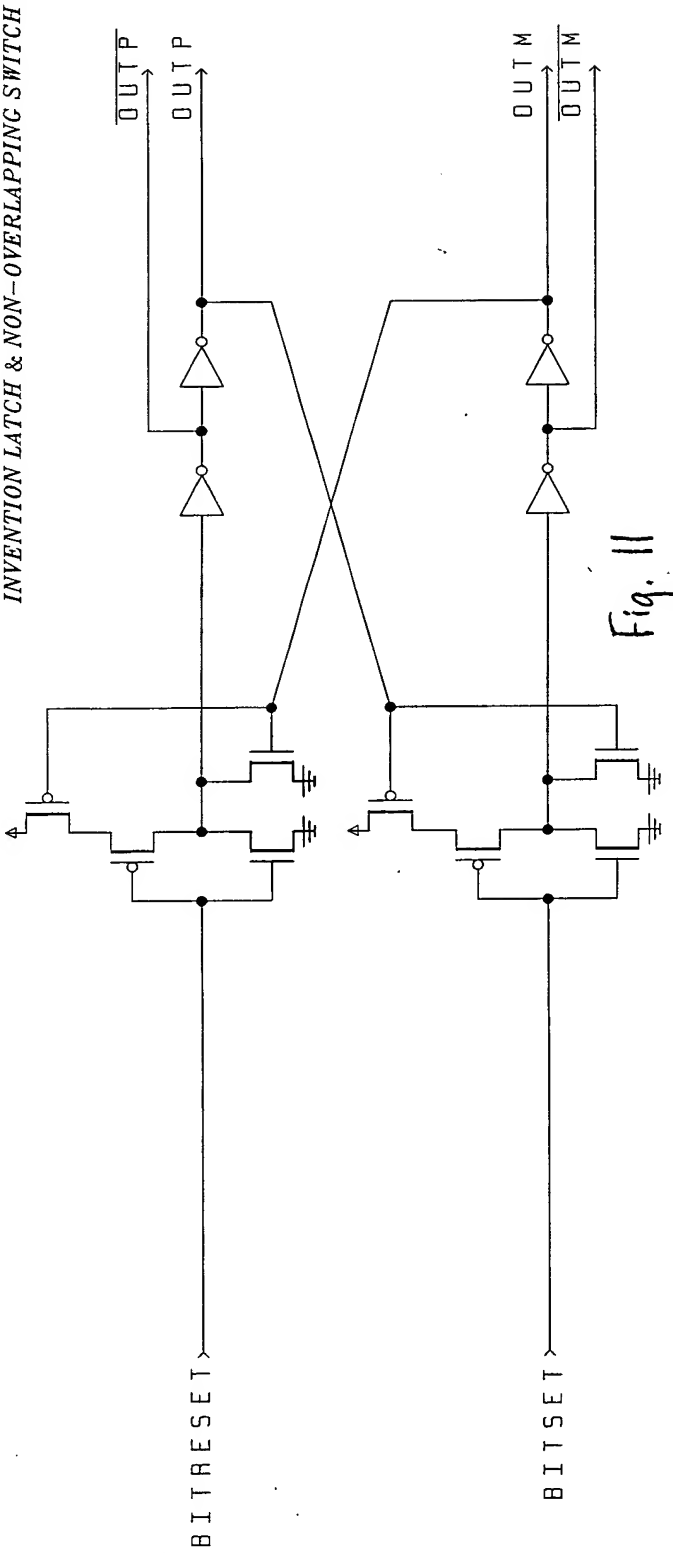

Fig. 11

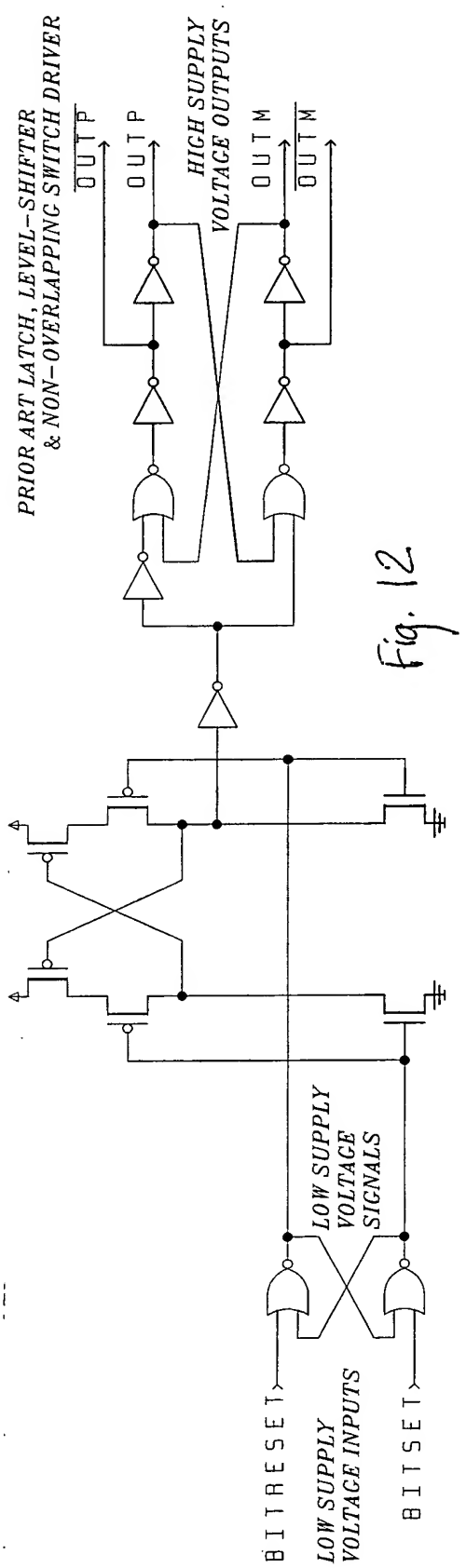
PRIOR ART LATCH, LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
HIGH SUPPLY VOLTAGE OUTPUTS
OUTM
OUTM
LOW SUPPLY VOLTAGE SIGNALS
BITRESET
LOW SUPPLY VOLTAGE INPUTS
BITSET

Fig. 12

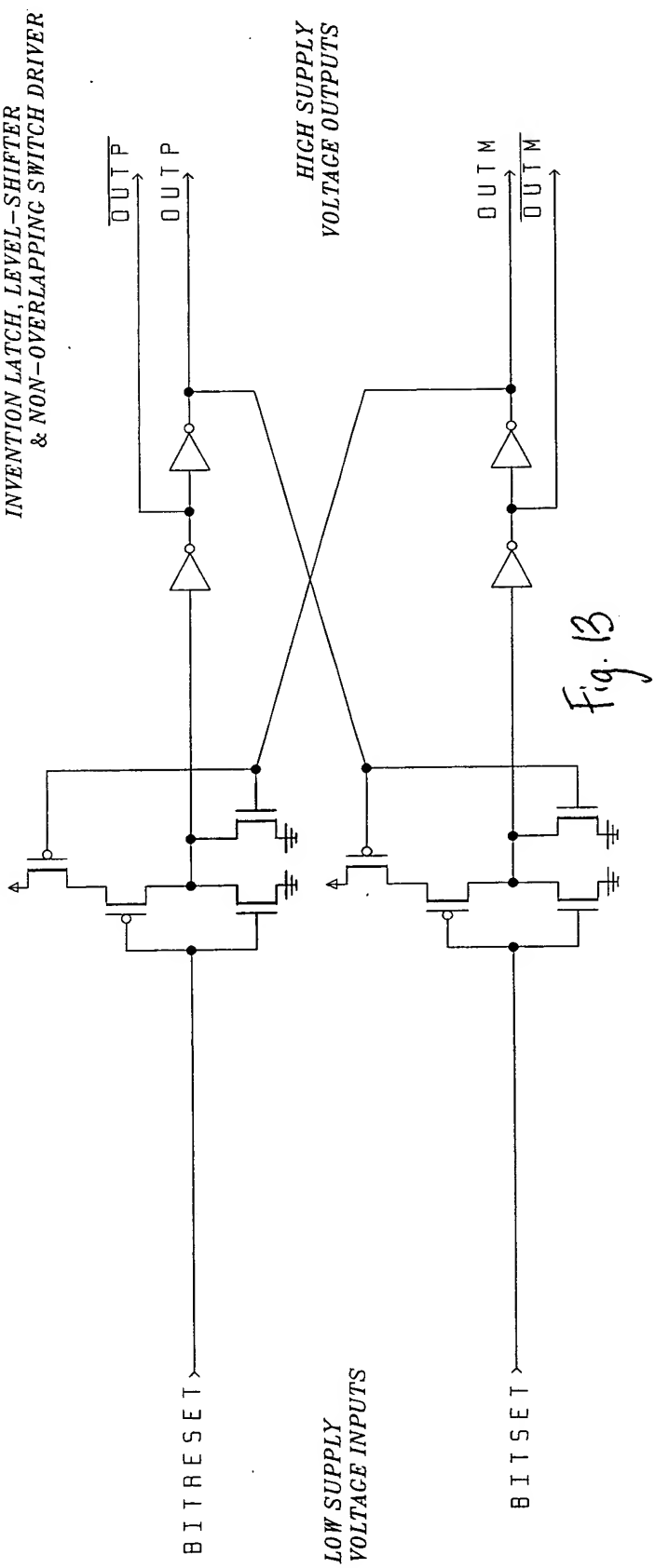
INVENTION LATCH, LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
HIGH SUPPLY VOLTAGE OUTPUTS
OUTM
OUTM
BITRESET
LOW SUPPLY VOLTAGE INPUTS
BITSET

Fig. 13